PATENT ABSTRACTS OF JAPAN

(11)Publication number : 2002-026027

(43)Date of publication of application : 25.01.2002

(51)Int.Cl. H01L 21/331
H01L 29/73
H01L 21/205
H01L 21/28
H01L 29/165
H01L 29/417

(21)Application number : 2000-199184

(22)Date of filing : 30.06.2000

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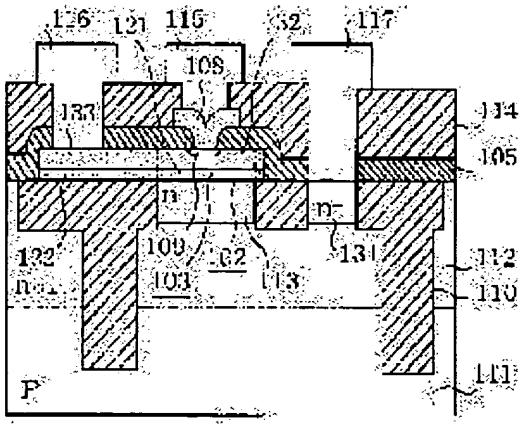
(54) SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a semiconductor device and its manufacturing method which forms an SiGe epitaxial growth layer for base regions on a silicon substrate and a polycrystalline SiGe film for outer base electrodes on an insulation (silicon oxide) film at the same time.

SOLUTION: The method of forming an SiGe film 103 on a semiconductor substrate 111 having an insulation film for element isolating regions, etc., comprises a step for forming a thin Si film 102 on the semiconductor substrate, depositing an SiGe film thereon, a step for epitaxially growing a single crystal Si film 121 and an SiGe film 132 on the semiconductor substrate surface, and a step for forming polycrystalline Si film 122 and an SiGe film 133 on the insulation film. Since the Si film is previously formed on the insulation film, the polycrystalline SiGe film is formed with a high adhesion also on the insulation film. Bipolar transistors are formed, each having a base region made from the SiGe/Si single crystal layer and an outer base electrode made from the SiGe/Si polycrystalline film.



LEGAL STATUS

[Date of request for examination] 07.01.2005

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] The manufacture approach of a semiconductor device is started, especially connection resistance forms the SiGe film advantageous to high-speed operation in the condition small enough, and this invention relates to the formation approach of the base region which becomes advantageous on electrical properties, such as a noise figure.
[0002]
[Description of the Prior Art] By using a low-temperature epitaxial grown method for device active regions, such as a base region of a bipolar component, the source / drain field of a CMOS device, and a channel field, and forming shallow junction in them in recent years, the device which realizes improvement in the speed and high integration is proposed, and it is in the way of utilization. The bipolar transistor and its manufacture approach of the conventional technique of such structure are explained. Drawing 10 thru/or drawing 13 show the production process sectional view of the conventional bipolar transistor, and drawing 9 is the sectional view of the bipolar transistor formed by the manufacture approach. As shown in drawing 9 , the semi-conductor substrate 11 consists of a p-type silicon substrate, and it has n mold impurity diffusion field 12 (n well) of high high impurity concentration, and n-impurity diffusion field 13 and the high concentration impurity diffusion field 131 which were formed in the impurity diffusion field 12. a trench forms in the principal plane of the semi-conductor substrate 11 -- having -- SiO2 etc. -- it fills up with an insulating material and the component isolation region 10 is formed. The front face of the component formation field surrounded by the component isolation region of semi-conductor substrate 11 principal plane is exposed. A bipolar transistor is formed in this semi-conductor substrate 11. First, the impurity diffusion field 13 and the high concentration impurity diffusion field 131 constitute the collector field.
[0003] The semi-conductor layer 2 is formed on the component isolation region 10 and the impurity diffusion field 13. On the component isolation region 10, the single-crystal-silicon layer 21 is formed on the polycrystalline silicon layer 22 and the impurity diffusion field 13, and these constitute the semi-conductor layer 2. The single-crystal-silicon layer 21 constitutes a base region, and n mold emitter region 9 is formed in the front face. The polycrystalline silicon layer 22 constitutes the external base electrode. The semi-conductor substrate 11 is covered with the insulator layers 5, such as a silicon nitride, and is further covered with the insulator layers 14, such as silicon oxide. The contact hole is formed in insulator layers 5 and 14, respectively so that the polycrystalline silicon layer 22, an emitter region 9, and the high concentration impurity diffusion field 131 may be exposed, respectively. The external base electrode 8 of polycrystalline silicon is formed in the contact hole which the emitter region 9 has exposed, and the emitter metal electrode 15 is formed on it. The base metal electrode 16 is formed in the contact hole which the polycrystalline silicon layer 22 of an external base electrode has exposed. And the collector metal electrode 17 is formed in the contact hole which the high concentration impurity diffusion field 131 has exposed.
[0004] Next, the manufacture approach of the bipolar transistor shown in drawing 9 is explained. First, the p-type silicon semi-conductor layer 2 containing boron (B) is formed of epitaxial growth on the semi-conductor substrate 11. On a component formation field, the base region 21 of p mold single crystal silicon is formed of this epitaxial growth, and p mold polycrystalline silicon layer 22 is formed

on the insulator layer of the component isolation region 10 of it. Patterning of this silicon semi-conductor layer 2 is carried out to a predetermined configuration (drawing 1010). And the silicon nitride (Si3 N4) 5 is deposited on the semi-conductor substrate 11 so that the silicon semi-conductor layer 2 may be covered (drawing 11). Opening 6 is formed in the part of the single-crystal-silicon layer (base region) 21 of the silicon nitride 5 by anisotropic etching, such as RIE (Reactive Ion Etching). At this time, the single-crystal-silicon layer 21 of a base region is exposed to opening 6 pars basilaris ossis occipitalis (drawing 12). Next, the polycrystalline silicon film is deposited all over the silicon nitride 5, and the ion implantation of the arsenic (As) is carried out to this polycrystalline silicon film.

[0005] n mold emitter region 9 is formed in the part which the base region 21 of the semi-conductor layer 2 was made to diffuse the arsenic in the polycrystalline silicon film, and was furthermore spread like the heat process. Furthermore, by anisotropic etching, such as RIE, patterning of the polycrystalline silicon film is carried out, and the emitter drawer electrode 8 is formed (drawing 13). Next, the interlayer insulation films 14, such as silicon oxide, are made to deposit on the emitter drawer electrode 8 and the silicon nitride 5, a contact hole is punctured to this interlayer insulation film 14, and the emitter drawer electrode 8 is exposed to it. And the emitter metal electrodes 15, such as aluminum which connects with this emitter drawer electrode 8 electrically, are formed. At this time, a contact hole is formed also in the polycrystalline silicon layer 22 of an external base electrode, and the silicon nitride 5 on the high concentration impurity diffusion field 131, and the base metal electrode 16 and the collector metal electrode 17 which are connected electrically are formed in the polycrystalline silicon layer 22 and the high concentration impurity diffusion field 131 of an external base electrode (drawing 9).

[0006]

[Problem(s) to be Solved by the Invention] Thus, although they consist of a single crystal field and a polycrystal field, since the base region of a single-crystal-silicon layer and the external base electrode of a polycrystalline silicon layer are formed at one process, they do not almost have the connection resistance between both fields, and a noise figure etc. is very advantageous [a base electrode] by the conventional manufacture approach, on an electrical property. Moreover, development of the SiGe heterojunction bipolar transistor which changed the base region into the SiGe film from Si film for the further improvement in the speed is performed. however -- if epitaxial growth of the SiGe film tends to be carried out by the same production process as Si bipolar transistor -- a silicon substrate top -- the SiGe growth film (single crystal) -- although formed easily, since the selection ratio is high, the polycrystal SiGe film is not formed to silicon oxide (since the uneven film is made even if formed, a membranous role is not made). Therefore, since the external base electrode on a component isolation region is not formed by this approach, the external base electrode which performs electrical installation of a base metal electrode and a base region cannot be formed.

[0007] Thus, when forming the SiGe epitaxial growth phase used as a base region on a silicon semi-conductor substrate, the work in which the polycrystal SiGe film used as an external base electrode is made to form on an insulator layer (silicon oxide) had to be carried out to coincidence. This invention is made according to such a situation, and when forming the SiGe epitaxial growth phase used as a base region on a silicon semi-conductor substrate, it provides coincidence with the manufacture approach of a semiconductor device and semiconductor device which make the polycrystal SiGe film used as an external base electrode form also on an insulator layer (silicon oxide).

[0008]

[Means for Solving the Problem] In the approach of forming the SiGe film on the semi-conductor substrate which has the insulator layer which was formed in the silicon substrate surface as a component isolation region etc., or was embedded, this invention forms thin Si film on this semi-conductor substrate, and the description is in making the SiGe film deposit on it. In a silicon substrate surface, the single crystal Si film and the SiGe film grow epitaxially, and the polycrystal Si film and the SiGe film are formed on an insulator layer. Since Si film is beforehand formed on the insulator layer, the polycrystal SiGe film is formed with high adhesion also on an insulator layer. Thus, if the SiGe hetero joint bipolar transistor which makes a base region the formed single crystal SiGe/Si epitaxial growth phase, and uses the polycrystal SiGe/Si film on an insulator layer as an external base electrode is constituted, there is almost no connection resistance with the external base electrode connected to a base region and a metal electrode, and it is very advantageous on electrical properties, such as a noise figure.

For making high-speed operation possible, a base region is changed into the SiGe film from Si film, there is almost no connection resistance with the external base electrode which gathers the passing speed of the electron in a base region and which follows a base region and this in this invention although it is required, and a very advantageous SiGe heterojunction bipolar transistor is offered on electrical properties, such as a noise figure.

[0009] Namely, the insulator layer embedded alternatively [the semiconductor device of this invention] to a silicon semi-conductor substrate and said semi-conductor substrate principal plane, The semi-conductor layer which consisted of SiGe layers formed on the substrate Si layer which was formed on said semi-conductor substrate principal plane and said insulator layer, and was directly formed in said semi-conductor substrate principal plane and said insulator layer, and this substrate Si layer is provided. Said semi-conductor layer is characterized by for the field formed on said semi-conductor substrate principal plane being a single crystal layer, and the field formed on said insulator layer being a polycrystal layer. By forming a bipolar transistor in said semi-conductor substrate, this bipolar transistor has the 1st conductivity-type collector field, and it has the 1st conductivity-type emitter region in the surface field of this 2nd conductivity-type base region, using said single crystal layer as the 2nd conductivity-type base region, and you may make it use said polycrystal layer as an external base electrode. You may make it the thickness of said substrate Si layer to the thickness of said semi-conductor layer be 10 - 20%. If a substrate Si layer is thin, an external base electrode will not be formed in homogeneity, if thick, resistance becomes high and the rapidity of a transistor cannot be expected. Therefore, the above-mentioned range is suitable. You may make it germanium content in said SiGe layer be below 15 atom %.

[0010] The process which forms the insulator layer by which the manufacture approach of the semiconductor device of this invention was embedded alternatively at the silicon semi-conductor substrate principal plane, The process which forms the semi-conductor layer by which the laminating of the SiGe layer was carried out one by one a substrate Si layer and on this on said semi-conductor substrate principal plane and said insulator layer is provided. Said semi-conductor layer It is characterized by for the field formed on said semi-conductor substrate principal plane being a single crystal layer, and the field formed on said insulator layer being a polycrystal layer. You may make it form continuously said substrate Si layer and SiGe layer by which the laminating was carried out within the same processor. The process which forms said semi-conductor layer is SiH4. The included gas is supplied, said substrate Si layer is formed, and it is GeH4 further after predetermined time progress. Gas is supplied and you may make it form said SiGe layer.

[0011]

[Embodiment of the Invention] Hereafter, the gestalt of implementation of invention is explained with reference to a drawing. First, the 1st example is explained with reference to drawing 1 thru/or drawing 7 . Drawing 6 and drawing 7 are process sectional views where the sectional view and the top view, drawing 2 , or drawing 5 of a semiconductor device (bipolar transistor) explains the manufacture approach of this semiconductor device. it is shown in drawing 6 and drawing 7 -- as -- the semi-conductor substrate 111 -- from a p-type silicon substrate -- becoming -- n mold impurity diffusion field 112 (n well) and n -- it has n-impurity diffusion field 113 and the high concentration impurity diffusion field 131 which were formed in the well 112. a trench (STI:Shallow Trench Isolation) forms in the principal plane of the semi-conductor substrate 111 -- having -- **** -- the inside of this -- SiO2 etc. -- it fills up with an insulating material and the component isolation region 110 is formed. This invention does not restrict the structure of a component isolation region to STI. LOCOS (LOCal Oxidation of Silicon) -- it is also possible to use the silicon oxide by law etc.

[0012] The front face of the component formation field surrounded by the component isolation region of semi-conductor substrate 111 principal plane is exposed. A bipolar transistor is formed in this semi-conductor substrate 111. First, the impurity diffusion field 113 and the high concentration impurity diffusion field 131 constitute the collector field. And on the component isolation region 110 and the impurity diffusion field 113, the semi-conductor layer to which the laminating of the Si film 102 and the SiGe film 103 was carried out is formed. On the component isolation region 110, the single crystal Si film 121 is formed on the polycrystal Si film 122 and the impurity diffusion field 113, and these constitute the Si film 102. On the polycrystal Si film 122, the single crystal SiGe film 132 is formed on the polycrystal SiGe film 133 and the single crystal Si film 121, and these constitute the SiGe film 103.

The single crystal Si film 121 and the single crystal SiGe film 132 on this constitute the base region, and n mold emitter region 109 is formed in that front face. And the polycrystal Si film 122 and the polycrystal SiGe film 133 on this constitute the external base electrode. The semi-conductor substrate 111 is covered with the insulator layers 105, such as a silicon nitride, and a it top is further covered with the insulator layers 114, such as silicon oxide.

[0013] The contact hole is formed in insulator layers 105 and 114, respectively so that the polycrystal SiGe film 133, an emitter region 109, and the high concentration impurity diffusion field 131 may be exposed, respectively. The emitter drawer electrode 108 of polycrystalline silicon is formed in the contact hole which the emitter region 109 has exposed, and the emitter metal electrodes 115, such as aluminum, are formed on it. The base metal electrodes 116, such as aluminum, are formed in the contact hole which the polycrystal SiGe film 133 which constitutes an external base electrode has exposed. And the collector metal electrodes 117, such as aluminum, are formed in the contact hole which the high concentration impurity diffusion field 131 has exposed.

[0014] Next, the manufacture approach of the bipolar transistor shown in drawing 6 and drawing 7 is explained. The semi-conductor layers 102 and 103 containing boron (B) are formed by the epitaxial grown method on the semi-conductor substrate 111. First, by this epitaxial grown method, on a component formation field, the p mold single crystal Si film 121 used as the base region whose thickness is about 10nm grows, and the p mold polycrystal Si film 122 of about 10nm of thickness is formed on the insulator layer (silicon oxide) of the component isolation region 110 (drawing 1). Then, the p mold single crystal SiGe film 132 of about 50-100nm of thickness grows on the p mold single crystal Si film 121 with this epitaxial grown method, and the p mold polycrystal SiGe film 133 whose thickness is about 50-100nm is formed on the p mold polycrystal Si film 122 (drawing 2 R> 2). Next, patterning of these semi-conductor layers 102 and 103 is carried out to a predetermined configuration so that a base region and a component isolation region may be covered. And the insulator layer 105 which consists of a silicon nitride (Si3 N4) so that the semi-conductor layers 102 and 103 by which patterning was carried out may be covered is made to deposit on the semi-conductor substrate 111 (drawing 3). Opening 106 is formed in the part of the single crystal SiGe film 132 of this insulator layer 105 by anisotropic etching, such as RIE (Reactive Ion Etching). At this time, the single crystal SiGe film 132 used as a base region is exposed to opening 106 pars basilaris ossis occipitalis (drawing 4).

[0015] Next, the polycrystalline silicon film is made to deposit all over an insulator layer 105, and the ion implantation of the arsenic (As) is carried out to this polycrystalline silicon film. n mold emitter region 109 is formed in the part which the single crystal SiGe film 132 was made to diffuse the arsenic in the polycrystalline silicon film, and was furthermore spread like the heat process. Furthermore, by anisotropic etching, such as RIE, patterning of the polycrystalline silicon film is carried out, and the emitter drawer electrode 108 is formed (drawing 5). Next, the interlayer insulation films 114, such as silicon oxide, are made to deposit on the emitter drawer electrode 108 and an insulator layer 105, a contact hole is punctured to this interlayer insulation film 114, and the emitter drawer electrode 108 is exposed to it. And the emitter metal electrodes 115, such as aluminum electrically connected to this emitter drawer electrode 108, are formed. At this time, a contact hole is formed also in the polycrystal SiGe film 133 and the insulator layer 105 on the high concentration impurity diffusion field 131, and the collector metal electrodes 117, such as the base metal electrodes 116, such as aluminum connected electrically, and aluminum, are formed in the polycrystal SiGe film 133 and the high concentration impurity diffusion field 131 (drawing 6 , drawing 7).

[0016] Next, the growth approach to the semi-conductor substrate of the semi-conductor layer which consists of SiGe/Si with reference to drawing 8 is explained. Drawing 8 R> 8 is the property Fig. showing the relation of the amount of supply of reactant gas and reaction time which are supplied to the reaction processing room in which the semi-conductor substrate was laid, an axis of ordinate expresses the flow rate of the gas supplied to a reaction processing room, and the axis of abscissa expresses reaction time (minute). This example has the description in carrying out laminating formation of the two semi-conductor layer components from which a class differs continuously at one reaction processing room. A two-layer semi-conductor layer is formed by the epitaxial grown method on a semi-conductor substrate (refer to drawing 6). First, a silicon semi-conductor substrate is laid in the susceptor of a reaction processing room. A reaction processing room is sealed, and first, silane (SiH4) gas is supplied at time of day A, and it continues passing until a reaction ends constant flow (v1). SiH4 Si film deposits

gas by the reaction shown in a degree type (1). the case where Si film is made to diffuse impurities, such as boron, at this time -- B-2 H6 [for example,] gas -- the specified quantity -- short-time supply is carried out.

[0017]

SiH4 ->Si+2H2 ... (1)

The thickness of Si film is set to about 10nm between the time amount t by time of day B. Formation of Si film is ended here. By this epitaxial grown method, on a component formation field, the p mold single crystal Si film used as the base region whose thickness is about 10nm grows, and the p mold polycrystal Si film of about 10nm of thickness is continuously formed on the insulator layer of a component isolation region with this. Then, the SiGe film is made to deposit with this epitaxial grown method. That is, it sets at time of day B, and is SiH4. It combines with supply of gas and is GeH4. Gas is supplied, and it continues passing until a reaction ends constant flow (v2). SiH4 Gas and GeH4 By supply of gas, as shown in a degree type (2), the SiGe film accumulates. the case where the SiGe film is made to diffuse impurities, such as boron, at this time -- B-2 H6 [for example,] gas -- the specified quantity -- short-time supply is carried out. Growth rates are about 30 nm/min (if the amount of supply of GeH4 is changed in practice, a growth rate will also change). Therefore, the formation time amount of Si film is about 20 seconds, and the formation time amount of the SiGe film is about 2 - 3 minutes. Moreover, for temperature, 600-700 degrees C and a pressure are [the growth conditions at this time] 10torr(s) and SiH4. A quantity of gas flow is 3 and GeH4 200cm. It is adjustable by the presentation which a quantity of gas flow aims at.

[0018]

SiH4+GeH4 ->SiGe+4H2 ... (2)

SiGe is Si1-x Gex in practice. It is expressed. In this invention, 0.15 or less are suitable for x. And it is possible by setting up suitably flow rate (v2/v1) to set the value of x as a predetermined value (expressed with x=v2/(v1+v2) and 1-x=v1/(v1+v2)). Thus, the p mold single crystal SiGe film of about 50-100nm of thickness grows on the p mold single crystal Si film of the lower layer (substrate) of a semi-conductor layer, and the p mold polycrystal SiGe film whose thickness is about 50-100nm is formed on the p mold polycrystal Si film formed at the insulator layer. Single crystal SiGe thickness expresses base width of face. This base region needs to make thickness of the SiGe film thin for base-transit-time compaction (namely, improvement in the speed). However, if it is made thin, pressure-proofing between C-E will fall. These both have the relation of a trade-off, and in order to obtain suitable relation, they are setting thickness to 50-100nm. As mentioned above, like an example, in a silicon substrate surface, the single crystal Si film and the SiGe film grow epitaxially, and the polycrystal Si film and the SiGe film are formed on an insulator layer. Since Si film is beforehand formed on the insulator layer, the polycrystal SiGe film is formed with high adhesion also on an insulator layer.

[0019]

[Effect of the Invention] As mentioned above, according to this invention, in a silicon substrate surface, the single crystal Si film and the SiGe film grow epitaxially, and the polycrystal Si film and the SiGe film are formed on an insulator layer. Since Si film is beforehand formed on the insulator layer as substrate film, the polycrystal SiGe film is formed with high adhesion also on an insulator layer. Thus, if the SiGe hetero joint bipolar transistor which makes a base region the formed single crystal SiGe/Si epitaxial growth phase, and uses the polycrystal SiGe/Si film on an insulator layer as an external base electrode is constituted, connection resistance with the external base electrode connected to a base region and a metal electrode is almost lost, and is very advantageous on electrical properties, such as a noise figure. In this invention, when connection resistance with a base region and the external base electrode following this decreases, while the high-speed operation of a transistor becomes possible, the area of a component field is reduced, clock frequency is high, and its thermal noise is low, and it becomes possible [forming a bipolar transistor with little power consumption] from the former.

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CLAIMS

[Claim(s)]
[Claim 1] A silicon semi-conductor substrate and the insulator layer embedded alternatively at said semi-conductor substrate principal plane, The semi-conductor layer which consisted of SiGe layers formed on the substrate Si layer which was formed on said semi-conductor substrate principal plane and said insulator layer, and was directly formed in said semi-conductor substrate principal plane and said insulator layer, and this substrate Si layer is provided. Said semi-conductor layer is a semiconductor device characterized by the field where the field formed on said semi-conductor substrate principal plane was formed on the single crystal layer and said insulator layer being a polycrystal layer.
[Claim 2] It is the semiconductor device according to claim 1 characterized by forming a bipolar transistor in said semi-conductor substrate, for this bipolar transistor having the 1st conductivity-type collector field, and having the 1st conductivity-type emitter region in the surface field of this 2nd conductivity-type base region, using said single crystal layer as the 2nd conductivity-type base region, and using said polycrystal layer as an external base electrode.
[Claim 3] The thickness of said substrate Si layer to the thickness of said semi-conductor layer is a semiconductor device according to claim 1 or 2 characterized by being 10 - 20%.
[Claim 4] germanium content in said SiGe layer is a semiconductor device according to claim 1 to 3 characterized by being below 15 atom %.
[Claim 5] It is the manufacture approach of the semiconductor device which possesses the process which forms the insulator layer embedded alternatively at the silicon semi-conductor substrate principal plane, and the process which form the semi-conductor layer by which the laminating of the SiGe layer was carried out one by one a substrate Si layer and on this on said semi-conductor substrate principal plane and said insulator layer, and is characterized by for the field where the field where said semi-conductor layer was formed on said semi-conductor substrate principal plane was formed on a single crystal layer and said insulator layer to be a polycrystal layer.
[Claim 6] Said substrate Si layer and SiGe layer by which the laminating was carried out are the manufacture process of the semiconductor device according to claim 5 characterized by forming continuously within the same processor.
[Claim 7] The process which forms said semi-conductor layer is SiH4. The included gas is supplied, said substrate Si layer is formed, and it is GeH4 further after predetermined time progress. Manufacture process of the semiconductor device according to claim 5 characterized by supplying gas and forming said SiGe layer.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The process sectional view showing the manufacture approach of the semiconductor device of this invention.
[Drawing 2] The process sectional view showing the manufacture approach of the semiconductor device of this invention.
[Drawing 3] The process sectional view showing the manufacture approach of the semiconductor device of this invention.
[Drawing 4] The process sectional view showing the manufacture approach of the semiconductor device of this invention.
[Drawing 5] The process sectional view showing the manufacture approach of the semiconductor device of this invention.
[Drawing 6] The sectional view of the semiconductor device of this invention.
[Drawing 7] The top view of the semiconductor device shown in drawing 6 .
[Drawing 8] The property Fig. showing the relation of the amount of supply of reactant gas and reaction time which are supplied to the reaction processing room in which the semi-conductor substrate was laid.
[Drawing 9] The process sectional view showing the manufacture approach of the conventional semiconductor device.
[Drawing 10] The process sectional view showing the manufacture approach of the conventional semiconductor device.
[Drawing 11] The process sectional view showing the manufacture approach of the conventional semiconductor device.
[Drawing 12] The process sectional view showing the manufacture approach of the conventional semiconductor device.
[Drawing 13] The process sectional view showing the manufacture approach of the conventional semiconductor device.
[Description of Notations]
2 ... Silicon semi-conductor layer 5 ... A silicon nitride, 6,106 ... Opening, 8,108 ... An emitter drawer electrode, 9,109 ... Emitter region, 10,110 ... A component isolation region, 11,111 ... Semi-conductor substrate, 12,112 ... n mold impurity diffusion field (n well), 13,113 ... n-impurity diffusion field, 14,114 ... An interlayer insulation film, 15,115 ... Emitter metal electrode, 16,116 ... A base metal electrode, 17,117 ... Collector metal electrode, 21 ... Single-crystal-silicon layer 22 ... Polycrystalline silicon layer, 102 ... Si film (semi-conductor layer) 103 ... SiGe film (semi-conductor layer), 105 ... Insulator layer 121 [131 / 133 ... Polycrystal SiGe film. / ... A high concentration impurity diffusion field, 132 ... Single crystal SiGe film] ... The single crystal Si film, 122 ... Polycrystal Si film

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